

# **Basic Studies in Microwave Sciences**

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Final Report

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## **A. Abstract**

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## **B. Patent applications and publications**

### **B 1. Provisional patent applications**

- a. Pingshan Wang, Chaojiang Li, "Integrated Picosecond Pulse Generator Circuit," Application No. 12/570,349, Patent application filed on Sept. 30, 2009
- b. Pingshan Wang and Chunrong Song, "Dielectric Spectrometer with planner nanofluidic channels," Application No. 61/229127, July 28<sup>th</sup>, 2009;

### **B 2. Peer reviewed journal publications**

- a. Chunrong Song and Pingshan Wang, "Fabrication of Sub-10 nm Planar Nanofluidic Channels through Native Oxide Etch and Anodic Wafer Bonding," *IEEE Transactions on Nanotechnology*, vol. 9, no. 2, pp. 138-141, 2010
- b. Hanqiao Zhang, Axel Hoffmann, Ralu Divan, and Pingshan Wang, "DC current effects on magnetization reversal properties of submicron-sized Permalloy patterns for RF devices" *Appl. Phys. Lett.* **95**, 232503 (2009); doi:10.1063/1.3271777
- c. Huan Zou, Hanqiao Zhang, Chunrong Song, George Thomas, Haibo Wang, Pingshan Wang, "Characterization and modeling of mitered coplanar waveguide bends on silicon substrates," *International Journal of Electronics*, 2010. DOI: 10.1080/00207211003646977.

### **B 3. Journal submission under review**

- a. Chunrong Song and Pingshan Wang, "High electric field effects on GHz dielectric properties of water measured with microwave microfluidic devices," *Review of Scientific Instruments*, first revision, under review
- b. Pingshan Wang, Haibo Wang, George Thomas, Yueran Gao, and Chaojiang Li, "A High-Speed Sample-and-Hold Circuit Based on Integrated Transmission Lines," *Analog Integrated Circuits and Signal Processing*, Under revision

### **B 4. Peer reviewed conference papers**

- a. Chunrong Song and Pingshan Wang, "A technique for 1-10 nm planar nanofluidic channel fabrication," *Proceedings of Materials Research Society 2009 Fall Meeting*, Boston, Nov. 30<sup>th</sup> – Dec. 4<sup>th</sup>, 2009

- b. C.S. Song and P. Wang, "DC Electrical Breakdown of Water in a Sub-Micron Planar Gap," *Proceedings of the 17th IEEE International Pulsed Power Conference*, Washington DC, June 29 thru July 2, 2009

**B 5. Abstract reviewed and accepted for conference presentations**

- a. Huan Zou, Yongtao Geng, Chaojiang Li, Pingshan Wang, "A comparison study of transmission line based on-chip pulse generation circuits," *IEEE International Power Modulator and High Voltage Conference*, May 23-27, 2010, Atlanta, GA
- b. Pingshan Wang<sup>1</sup>, Yongtao Geng<sup>1</sup>, Huan Zou<sup>1</sup>, Haibo Wang<sup>2</sup>, Chaojiang Li, "An on-chip power modulator," *IEEE International Power Modulator and High Voltage Conference*, May 23-27, 2010, Atlanta, GA

**B 6. Other support that was based on the work in this project**

- a. NSF, award number: 0925424, "Broadband dielectric spectrometers with 1-10 nm planar nanofluidic channels," ECCS · INTEGRATIVE, HYBRD & COMPLX SY, 08/15/2009-08/14/12 (\$324,060)

## C. Technical results

### C 1. DI water dielectric properties under high intensity electric fields

Two types of microwave microfluidics devices are fabricated for broadband DI water dielectric property studies. The first type has metallic electrodes and is shown in Figs. 1(a)-(c). Fig. 1(d) shows typical measured results. It shows that breakdown happens when the applied DC electric field is  $\sim 100$  kV/cm. At the same time, water dielectric properties are not changed compared with water properties without DC electric fields. We are still working to understand the physical mechanisms of the breakdown (It is suspected that surface roughness played a role). New devices, which have much better surface smoothness with different electrode materials, are under fabrication for further water breakdown mechanism studies.

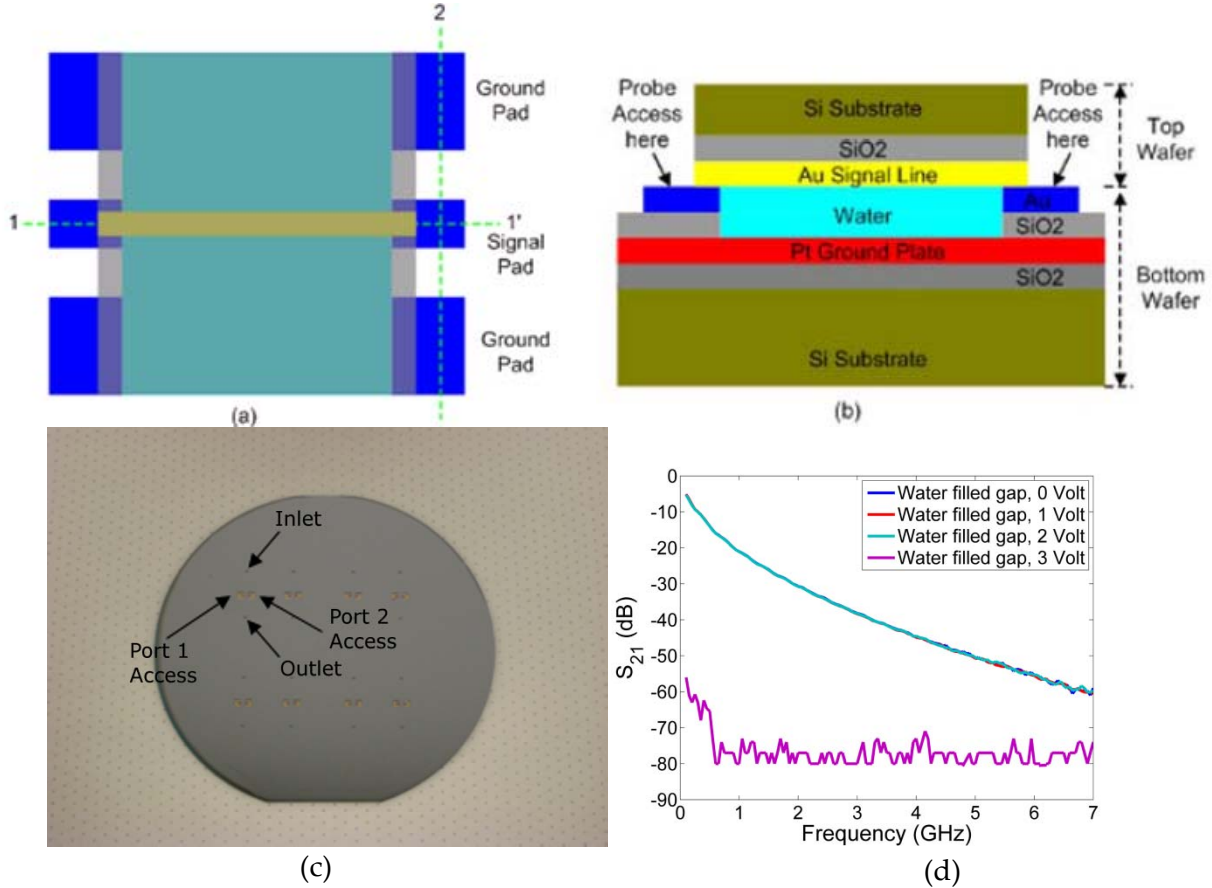


Fig. 1 (a) Top view illustration of the device. (b) Cross section view illustration at plane 1-1' in (a). (c) A photo of the bonded devices. Openings on top wafer are for probe access (Port 1 and Port 2) and inlet/outlet of water injection. (d) Measured  $S_{21}$  magnitude for different applied voltages.

The second type of devices has layouts similar to those of the first type. However, the electrodes and microwave transmission lines are from heavily doped silicon substrate. As a result, electrode surfaces are atomically flat. At the same time, metal Au and Pt are avoided since both are prone to electrolysis, which is suspected to be involved in water breakdown. Fig. 2(a) shows a photo of the fabricated microwave microfluidic device for water dielectric property characterization. Fig. 2(b) shows the atomically flat electrode surfaces.

Water property measurements are conducted with the system shown in Fig. 3. The measured water dielectric properties under different DC voltages (i.e. electric fields) are shown in Figs. 2(c) and (d). This is the first time to measure DI water permittivity under a DC field around 1 MV/cm. It shows that significant permittivity reduction occurs when the applied DC voltage is high. We are working to understand the physics behind the permittivity change.

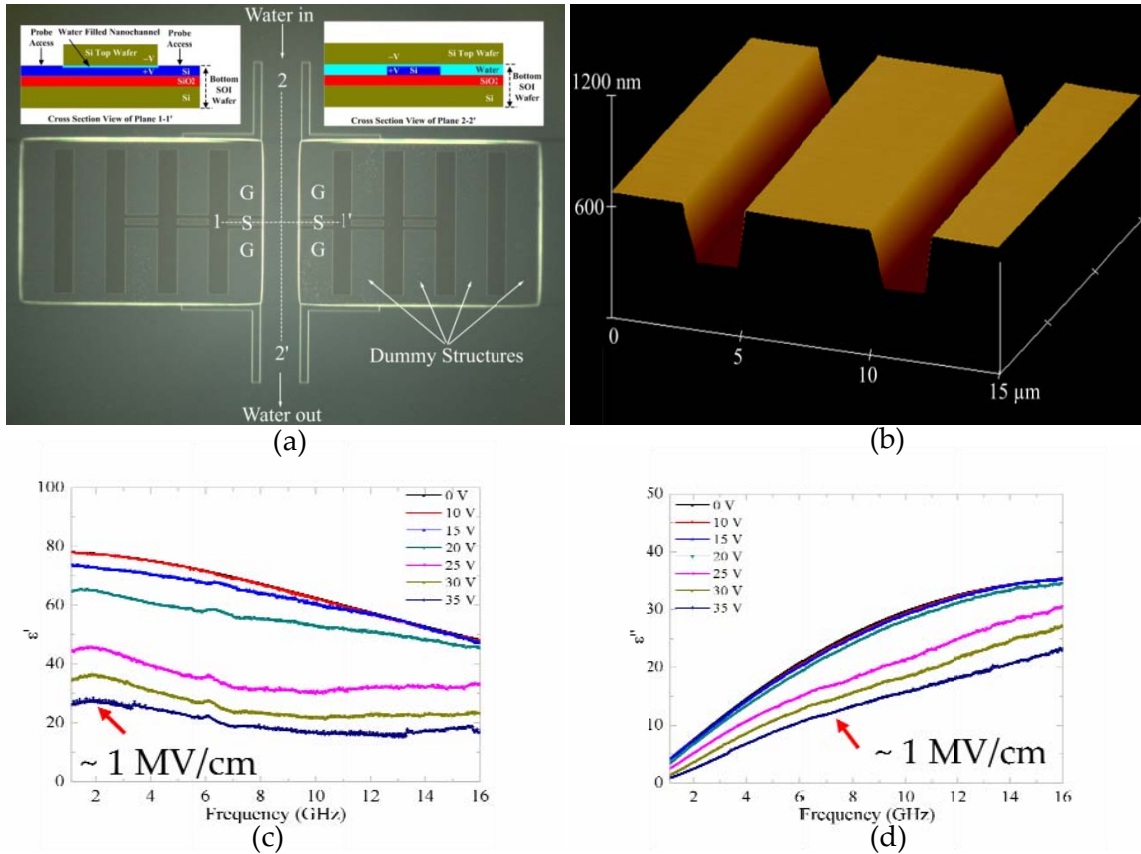


Fig. 2 (a) A picture of the fabricated microwave microfluidic devices. (b) An AFM picture shows atomically smooth device surface. (c) The real part and (d) the imaginary part of water dielectric properties under different applied DC voltages.

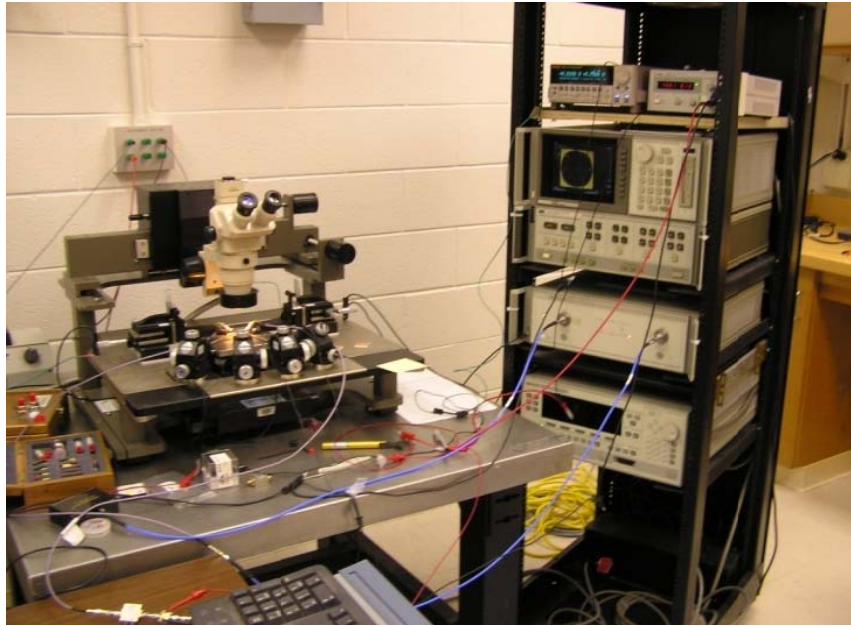


Fig. 3 A picture of the measurement system with an HP 8510 C network analyzer and a Cascade Microtech probe station.

Planar nanofluidic channels are also fabricated for water property studies. Fig. 4 shows a device with 15 nm channel height. Channels with 6 nm height have been obtained. New nano-channels are fabricated for confined DI water property measurements.

(a)

Planar nanofluidic channels for water property investigations. Due to extremely low voltage ( $< 1$  V) requirement for high field intensity, water electrolysis can be avoided.

(b)

Fig. 4 (a) A picture of 15 nm planar channels for water wetting process studies. (b) An AFM picture of a 6 nm planar channel.



## C 2. On-chip short pulse measurements

Circuit modules and circuits are designed and analyzed for on-chip short-pulse measurements. Figs. 5 (a) and (b) Show the circuit schematic and circuit micrograph in IBM 0.13  $\mu\text{m}$  CMOS technology. Figs. 5(c) and (d) show an input triangular pulse and the output pulse which is reconstructed from the circuit outputs, respectively. It shows the circuit is capable of capturing the shape of the 50 ps input pulse.

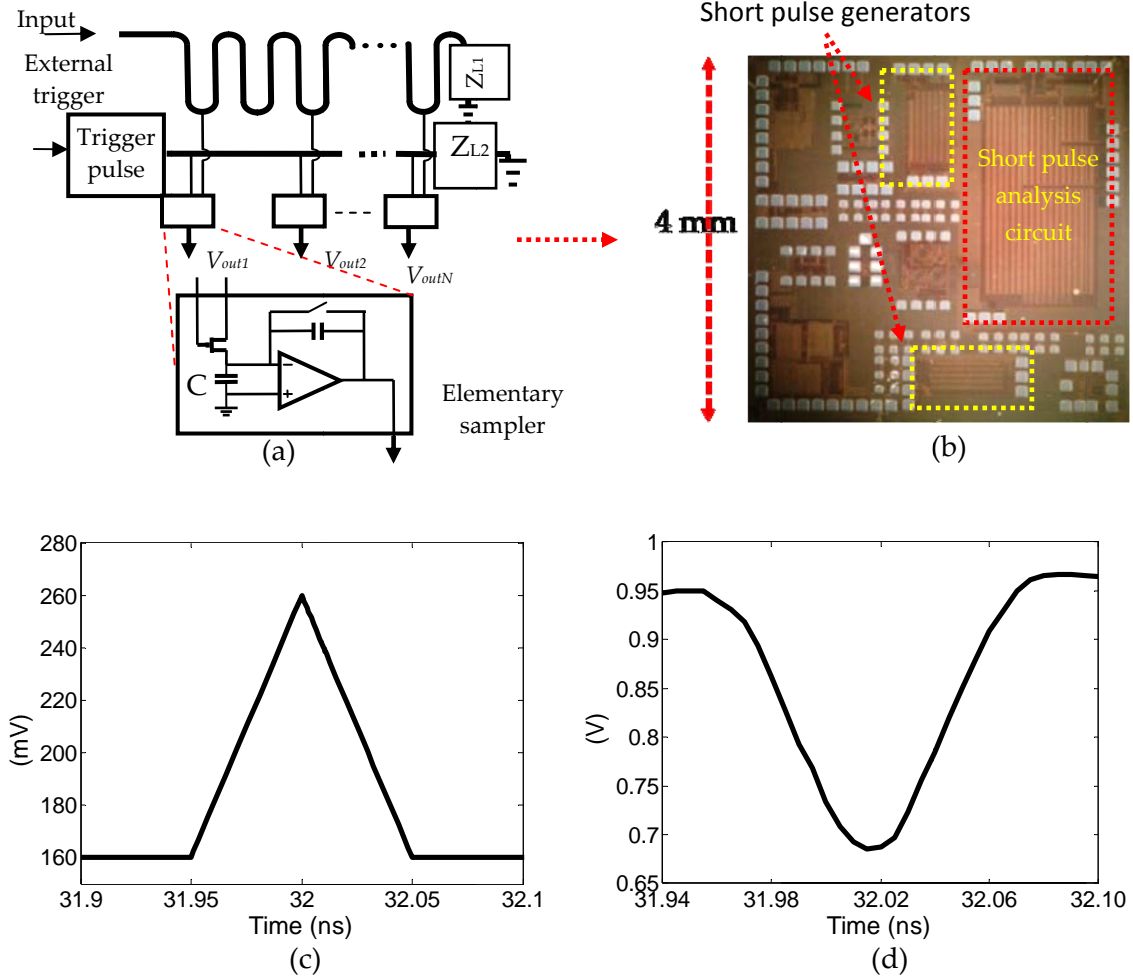


Fig. 5 (a) Schematic of the proposed CMOS circuit for on-chip short pulse capture and analysis. (b) A circuit micrograph of the circuit. (c) An input triangle pulse which is 50 ps wide (full width at half maximum, FWHM). (d) The output signal from the proposed circuit (post-layout simulation).

The meander line used to store the short pulse in the circuit (Figs. 5 (a) and (b)) is analyzed and modeled. Fig. 6 shows the CMOS meander line and the modeling results.

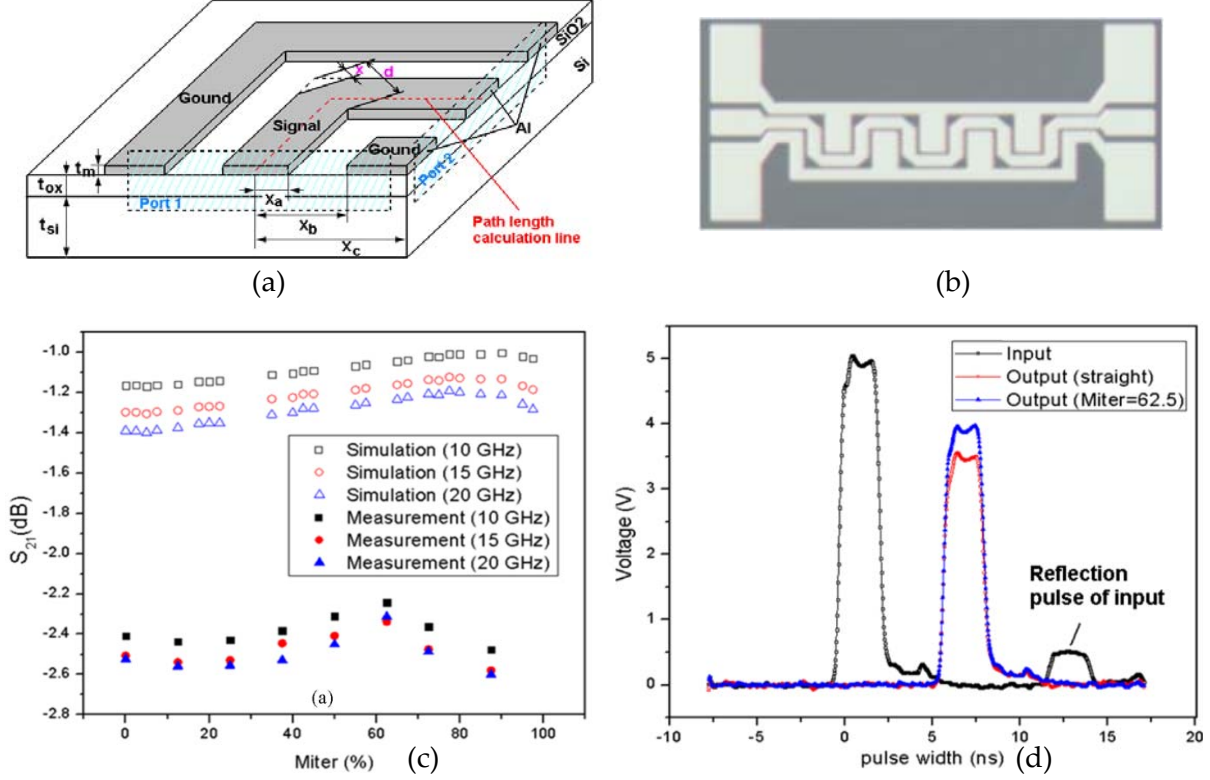


Fig. 6 (a) Illustration of a meander CMOS CPW line bend. (b) Photos of a fabricated test samples with Miter=50%. (c) Measured and simulated signal transmission coefficients for different miter ratios. The  $\sim 1.2$  dB difference is caused by measurement contact. (d) Measured pulse transmission through a meander CPW line. The results show that meander lines can transmit signals without significant signal deformation.

The trigger pulse generator in Fig. 5(a) is also used to generate picosecond short pulses with on-chip 4 mm long CMOS transmission lines, shown in Fig. 7(a) and Fig. 5(b). A slow input pulse,  $V_{in}$ , is converted to a short pulse to trigger the switch, an N-FET. The electrical length ( $\tau_p$ ) of the CMOS transmission line determines the output pulse duration ( $2 \times \tau_p$ ), shown in Fig. 7(b). The output pulse amplitude is ideally  $V_{DC}/2$ . The bandwidth of the used oscilloscope (which has an instantaneous bandwidth of 3.3 GHz) and the loss of the measurement connections (including cables etc.) are the main reasons for longer pulse durations and smaller pulse amplitudes in Fig. 7(b).

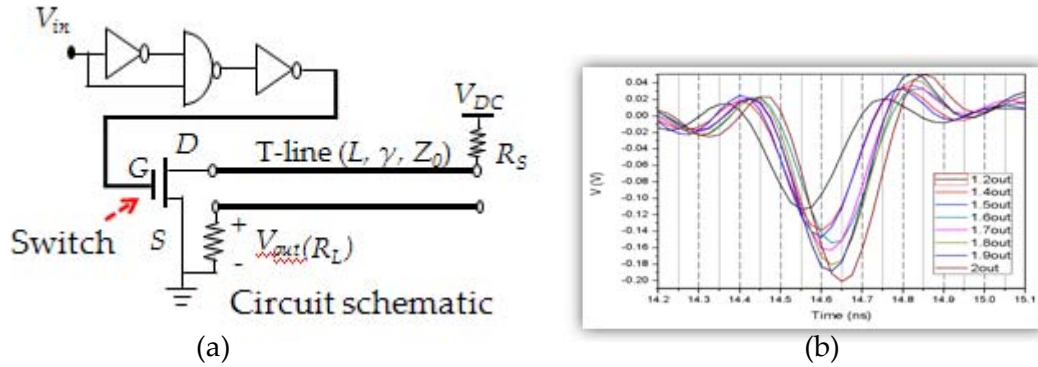


Fig. 7 (a) Schematic of a CMOS pulse generator based on a CMOS transmission line. The circuits (pulse generators) are shown in Fig. 5(b). (b) Measured output voltage pulses,  $V_{out}$ , for different applied  $V_{DC}$ .

#### D. Current and future work

Even though we have made great progress in our research, there is no end to any scientific and technology research. We are continuing the research work started in this project. The following activities are expected to generate exciting results in the near future.

- a. DI water breakdown mechanism research and confined water properties.
- b. CMOS high-voltage pulse generation and short pulse generation circuits.